WEST Search History

DATE: Tuesday, February 04, 2003

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L35	(adjust$4 or alter$4 or chang$4 or modif$7) near3 (operating adj2 (speed or rate)) near3 peripheral	4	L35
L34	l30 same L32	9	L34
L33	l30 and L32	11	L33
L32	(adjust$4 or alter$4 or chang$4 or modif$7) near3 (speed or rate) near3 peripheral	1153	L32
L31	l29 and L30	6	L31
L30	(detect$4 or sens$4) adj3 (speed or rate) adj3 peripheral	67	L30
L29	(high adj2 (rate or speed)) same (low adj2 (speed or rate)) same peripheral	1427	L29
L28	(set$4 adj3 clock adj3 (rate or speed) adj3 peripheral)	1	L28
L27	l23 same l21	3	L27
L26	L25 and l18	0	L26
L25	L23.ab.	52	L25
L24	l18 and L23	11	L24
L23	(select$4 or choos$4) near3 (rate or speed) near3 peripheral	398	L23
L22	l1 same L21	4	L22
L21	((based or depend$4 or respons$5) near3 condition)	191177	L21
L20	l8 and L18	3	L20
L19	l1 and L18	3	L19
L18	l12 or l13 or l14 or l15 or l16 or L17	1504	L18
L17	(((710/60)!.CCLS.))	210	L17
L16	(((710/18)!.CCLS.))	199	L16
L15	(((710/16)!.CCLS.))	176	L15
L14	(((710/15)!.CCLS.))	304	L14
L13	(((710/14)!.CCLS.))	249	L13
L12	((710/8)!.CCLS.)	639	L12
L11	l8 not l10	19	L11
L10	l8.ab.	7	L10
L9	l7 and L8	1	L9
L8	(adjust$4 or alter$4 or chang$4 or modif$7) near3 (speed or rate) near3 (peripheral adj2 device)	26	L8
L7	((based or depend$4 or respons$5) near3 (predefined or predetermined) near3 condition)	6911	L7

L6	L2.clm.	11	L6
L5	L2.ab.	27	L5
L4	L2 same state	8	L4
L3	L2 same condition	10	L3
L2	L1 same (respon$5 or based or depend$3)	93	L2
L1	(adjust$4 or alter$4 or chang$4 or modif$7) near3 (speed or rate) near3 ((peripheral or (i o) or (input output)) adj2 device)	302	L1

END OF SEARCH HISTORY

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L10: Entry 3 of 7 File: JPAB May 1, 1989

DOCUMENT-IDENTIFIER: JP 01112335 A
TITLE: ELECTRONIC EQUIPMENT

Abstract (2):
CONSTITUTION: A chip select signal from an address decoder 15 is also inputted to an access control circuit 12. The response speed of each of the peripheral circuits 11a, 11b... for the access of a CPU 10 that is the main control circuit is set differently from each other. The access control circuit 12 decides to which peripheral circuit the access is made, and adjusts the clock speed of the CPU 10 corresponding to a decided result via an access control signal 3. In such a way, it is not required to change the software of the main control circuit even when the synchronizing signal of the main control circuit is accelerated since the reference synchronizing signal of the main control circuit is changed corresponding to the response speed of a peripheral device automatically by hardware.

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L10: Entry 3 of 7 File: JPAB May 1, 1989

PUB-NO: JP401112335A
DOCUMENT-IDENTIFIER: JP 01112335 A
TITLE: ELECTRONIC EQUIPMENT

PUBN-DATE: May 1, 1989

INVENTOR-INFORMATION:
NAME COUNTRY
TANAHASHI, JUNICHI

ASSIGNEE-INFORMATION:
NAME COUNTRY
CANON INC

APPL-NO: JP62269292
APPL-DATE: October 27, 1987

INT-CL (IPC): G06F 9/30; G06F 1/04; G06F 13/42

ABSTRACT:

PURPOSE: To automatically perform the speed change of a reference synchronizing signal in a main control circuit corresponding to the speed of peripheral circuits by controlling the speed of the reference synchronizing signal in the main control circuit by detecting the access of the main control circuit to each peripheral circuit.

CONSTITUTION: A chip select signal from an address decoder 15 is also inputted to an access control circuit 12. The response speed of each of the peripheral circuits 11a, 11b... for the access of a CPU 10 that is the main control circuit is set differently from each other. The access control circuit 12 decides to which peripheral circuit the access is made, and adjusts the clock speed of the CPU 10 corresponding to a decided result via an access control signal 3. In such a way, it is not required to change the software of the main control circuit even when the synchronizing signal of the main control circuit is accelerated since the reference synchronizing signal of the main control circuit is changed corresponding to the response speed of a peripheral device automatically by hardware.

L11: Entry 1 of 19 File: USPT Sep 10, 2002

DOCUMENT-IDENTIFIER: US 6449663 B1
TITLE: Method and apparatus for adjusting an interval of polling a network printer based on changes in working status of the network printer

Brief Summary Text (11):
The prior art, however, provides fixed algorithms for polling peripheral devices without allowing the frequency of polling the peripheral device to vary as the need to monitor the peripheral device varies. Therefore, a need exists for adjusting the rate of polling peripheral devices as the need to monitor the peripheral device changes.

L11: Entry 4 of 19 File: USPT Aug 17, 1999

DOCUMENT-IDENTIFIER: US 5938742 A
TITLE: Method for configuring an intelligent low power serial bus

Detailed Description Text (248):
Bus dispatch master 1603 is the master of IDCS bus 150 and the source of all bus commands that result in data transfer. Bus dispatch master 1603 triggers the creation of command sequences by command sequencer 1612 in response to requests from IDCS bus client 1604 and peripheral client 1605, that are described below. In addition, bus dispatch master 1603 constantly monitors IDCS 150 and initiates command sequences to handle peripheral attachment and removal and interrupt requests (IRQs) from peripheral devices on IDCS bus 150. Bus dispatch master 1603 also senses and adjusts data rates to peripheral devices and enforces isochronous data transfer when required.

L11: Entry 9 of 19 File: USPT Aug 4, 1998

DOCUMENT-IDENTIFIER: US 5790536 A
TITLE: Hierarchical communication system providing intelligent data, program and processing migration

Detailed Description Text (294):
More specifically, FIG. 35 is a block diagram which illustrates a protocol 3301 used by a destination peripheral LAN device and a corresponding protocol 3303 used by a source peripheral LAN device to adjust the data rate and possibly the power level for future transmission between the two devices. At a block 3311, upon receiving a transmission from a source device, the destination device identifies a range value at a block 3313. In a low cost embodiment, the range value is identified by considering the received signal strength indications (RSSI) of the incoming transmission. Although RSSI circuitry might be placed in all peripheral LAN radios, the added expense may require that only peripheral LAN master devices receive the circuitry. This would mean that only peripheral LAN master devices would perform the function of the destination device. Other ranging techniques or signal quality assessments can also be used, such as measuring jitter in received signals, by adding additional functionality to the radios. Finally, after identifying the range value at the block 3313, the destination device subsequently transmits the range value to the slave device from which the transmission was received, at a block 3314.

L11: Entry 16 of 19 File: USPT Nov 26, 1996

DOCUMENT-IDENTIFIER: US 5579531 A
TITLE: System for selecting path among plurality of paths using plurality of multiplexers coupled to common bus to transfer data between peripheral devices and external device

Detailed Description Text (13):
In the above Embodiment 1, the peripheral devices are interconnected by the event buses to improve processing speed and response speed, and to facilitate changes in the interconnection of the peripheral devices. Another preferred embodiment of the present invention shown in FIG. 6 makes it possible to reduce the number of terminals according to the same idea as the first embodiment. The same reference symbols as those in FIG. 19 of the prior art designate the same or corresponding elements, and their description is omitted. In the figure, reference symbol 7b represents event buses as a plurality of signal transmission means for transmitting signals between a plurality of peripheral devices and a plurality of external terminals, and consists of three signal lines EV1, EV2 and EV3 like Embodiment 1. 12a to 17a represent multiplexers (MUX 1) as connection switch means for selectively connecting a plurality of the peripheral devices or a plurality of the external terminals with a plurality of the signal transmission means. The multiplexers 12a to 15a connect the terminals IN or OUT of the peripheral devices 2 and 3 to one of the signal lines of the event buses 7a, and the multiplexers 16a and 17a connect the general-purpose input/output external terminals A and B to one of the signal lines of the event buses 7b. Each multiplexer (MUX 1) has the same structure as shown in FIG. 2 of Embodiment 1.

L24: Entry 5 of 11 File: USPT Jul 13, 1999

DOCUMENT-IDENTIFIER: US 5922056 A
TITLE: Computer system with peripheral device characteristic sensing and automatic communications speed setting

Detailed Description Text (28):
However, if query 404 finds one or more unused addresses of the port 202, a process begins to check the port 202 for the possible addition of new devices. According to the present invention, the port 202 can select from multiple different speeds for communications with the attached peripheral devices. At any one time, all attached devices communicate with the port 202 at the same speed. For ease of explanation, the port 202 of the present example uses two different communication speeds: (1) a "faster" mode at 2 Mpbs, and/or (2) a "slower" mode at 1 Mpbs. The invention is not limited to two modes of communication, however. Three or more speeds may be used; the port 202 and peripheral devices, for example, may also support an additional communications mode using 4 Mbps.

Current US Original Classification (1):
710/16

End of Result Set

L24: Entry 11 of 11 File: USPT Apr 13, 1976

DOCUMENT-IDENTIFIER: US 3950735 A
TITLE: Method and apparatus for dynamically controlling read/write operations in a peripheral subsystem

Current US Original Classification (1):
710/60

CLAIMS:

4. In a data processing system which includes a central processing unit for issuing commands, a peripheral subsystem comprising

a plurality of peripheral devices, each of which operates at some speed to record or reproduce data each time a strobe pulse is received, and each of which includes means responsive to an interrogation signal for producing a speed constant signal specifying the operating speed of the device,

means responsive to a command issued by said central processing unit for applying an interrogation signal to a selected one of the peripheral devices to cause the selected device to produce a speed constant signal,

means for storing density information received in a command from the central processing unit and for storing the speed constant signal produced by the selected peripheral device, said density information specifying the density of data to be applied to or read from the selected peripheral device,

a memory for storing a plurality of data rate indices at different locations in the memory,

means for combining the density information and the speed constant signal to obtain a resultant identifying a location in said memory containing one of said data rate indices,

means for retrieving said one data rate index from the identified location in said memory, and

means for applying strobe pulses to the selected peripheral device at intervals defined by said one data rate index for execution of said commands.

9. In a data processing system comprising a central processing unit for issuing commands, a plurality of peripheral devices, each for recording and reproducing data and for producing a speed constant signal specifying the operating speed of the device, and a peripheral control unit for transferring data between the central processing unit and the peripheral devices in response to the commands from the central processing unit, a method of applying data to and reading data from the peripheral devices at differing rates depending upon the selected device comprising the steps of

a. supplying to the peripheral control unit a command coming from the central processing unit which identifies a particular peripheral device,

b. applying an interrogation signal from the peripheral control unit to the particular peripheral device identified in the command,

c. transmitting a speed constant signal to the peripheral control unit from the particular peripheral device, and

d. applying data to or reading data from the particular peripheral device under control of the peripheral control unit and at a rate determined by the speed constant signal supplied by the particular peripheral device for execution of said commands wherein step (d) further comprises

10. In a data processing system comprising a central processing unit, a plurality of peripheral devices, and a peripheral control unit interconnecting the central processing unit and the peripheral devices, a method of transferring data between the peripheral control unit and the peripheral devices at differing rates depending upon the selected device comprising the steps of

a. transmitting density information from the central processing unit to the peripheral control unit specifying the density of data to be transferred between the peripheral control unit and a selected peripheral device,

b. applying an interrogation signal from the peripheral control unit to the selected peripheral device,

c. transmitting from the selected peripheral device to the peripheral control unit a speed constant signal,

d. storing a plurality of data rate indices at different locations in a memory located within the peripheral control unit,

e. combining the density information and the speed constant signal to obtain a resultant which identifies a location in the memory containing one of the data rate indices, and

f. transferring data between the selected peripheral device and the peripheral control unit for execution of said commands at a rate defined by the data rate index contained in the identified memory location.

L5: Entry 6 of 27 File: JPAB Nov 11, 1997

PUB-NO: JP409294202A
DOCUMENT-IDENTIFIER: JP 09294202 A
TITLE: FACSIMILE EQUIPMENT

PUBN-DATE: November 11, 1997

INVENTOR-INFORMATION:
NAME COUNTRY
YOSHIDA, TAKEHIRO

ASSIGNEE-INFORMATION:
NAME COUNTRY
CANON INC

APPL-NO: JP08127824
APPL-DATE: April 24, 1996

INT-CL (IPC): H04 N 1/32; H04 N 1/21

ABSTRACT:

PROBLEM TO BE SOLVED: To allow the facsimile equipment to read data at a preferable speed to the equipment when transmission operation is not frequent and to read data at a highest speed in the case that transmission is frequent by changing a processing speed of an input output device based on the frequency of memory storage so as to use a plurality of lines.

SOLUTION: A control circuit 20 controls the entire facsimile equipment to change a read speed based on a frequency of memory storage. Concretely, when memory storage is frequent, the read speed is increased. When memory storage is less frequent, the read speed slows down. When a speed priority lamp 28 is lighted, the read speed is increased independently of the frequency of memory storage. Furthermore, whether or not the storage operation is discriminated for 20min or over is discriminated for past 30min and when the storage is conducted for 20min or over, since it means that the memory storage for transmission is conducted frequently, the processing speed of the input/output device is increased to read data at a highest speed in response to needs of the user.

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L4: Entry 6 of 8 File: DWPI Apr 21, 1998

DERWENT-ACC-NO: 1998-293663
DERWENT-WEEK: 199826

TITLE: Control apparatus for automatic transmission - has speed-change switching unit that switches between two speed-change modes, from which first and second range positions are attained by shift lever, during setting of speed-change mode switching condition

PATENT-ASSIGNEE:

ASSIGNEE	CODE
MATSUDA KK	MAZD

PRIORITY-DATA: 1996JP-0259459 (September 30, 1996)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 10103457 A	April 21, 1998		012	F16H059/08

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
JP 10103457A	September 30, 1996	1996JP-0259459	

INT-CL (IPC): B60 K 20/02; F16 H 59/08

ABSTRACTED-PUB-NO: JP 10103457A
BASIC-ABSTRACT:

The apparatus has a first output device which provides a speed-change signal based on a speed-change characteristic set up beforehand. The operation state of a shift lever (10) is detected by a shift-up or a shift-down command detecting switch (86,87). A second output device provides a speed-change signal based on the determined operation state of the shift lever. A speed change is performed by an executing device based on the output speed-change signals from both output devices.

The shift lever attains a first or a second range position by shifting to a first speed-change mode or between the first and second speed-change modes when performing the speed change based on the speed-change signal from the first output device or second output device, respectively. During the predetermined speed-change mode switching condition setting, a speed-change mode switching unit switches between the first and second speed-change modes.

ADVANTAGE - Enables quick and simple switching between speed-change modes when performing automatic speed change. Offers reliable speed-change control and high utilisation efficiency. Provides safety by enabling suitable gear ratio based on control mode.

CHOSEN-DRAWING: Dwg.2/13

TITLE-TERMS: CONTROL APPARATUS AUTOMATIC TRANSMISSION SPEED CHANGE SWITCH UNIT SWITCH TWO SPEED CHANGE MODE FIRST SECOND RANGE POSITION ATTAIN SHIFT LEVER SET

SPEED CHANGE MODE SWITCH CONDITION

DERWENT-CLASS: Q13 Q64 X22

EPI-CODES: X22-G01A;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1998-230864